IN THE CLAIMS:

Please cancel claims 20-22:

1. (Previously Presented) A memory device, comprising:

a buffer memory having a plurality of addressable memory registers;

a counter having a plurality of storage registers;

a logic network for writing and reading data into and out of said buffer memory, said logic network for partitioning said buffer memory into a plurality of buffer regions, wherein said logic network writes and reads data from a plurality of data classes into said plurality of buffer regions such that each data class is written into and read from a different buffer region, and wherein said logic network increments a storage register associated with a buffer region each time that buffer region reaches a predetermined usage level; and

a timer for periodically sending a timing signal to said logic network;

wherein in response to said timing signal said logic network recalls data from said counter registers and re-partitions said buffer memory such that a more utilized buffer region is assigned more addressable memory registers.

2. (Original) A memory device according to claim 1 wherein said logic network assigns a buffer region that is used less often fewer addressable memory registers.

3. (Original) A memory device according to claim 1 wherein each buffer region is always assigned at least a minimum number of addressable memory registers.

4. (Original) A memory device according to claim 1 wherein said predetermined usage level is full.

5. (Previously Presented) A memory device according to claim 1 wherein when a least used buffer region is assigned a minimum number of addressable memory registers the logic network assigns a buffer region that is less often fully utilized but that has more than the minimum number of addressable memory registers.

6. (Original) A memory device according to claim 1 wherein said data classes represent virtual lanes.

7. (Previously Presented) A memory device according to claim 1 wherein said timing signal initiates clearing of said plurality of storage registers.

8. (Previously Presented) A switch network comprising:

a network switch;

a card adaptor for transmitting and receiving data from said network switch, and

a memory device for storing data for and from said card adaptor, said memory having:

a buffer memory having a plurality of addressable memory registers;

a counter having a plurality of storage registers;

a logic network for writing and reading data into and out of said buffer memory, said logic network for partitioning said buffer memory into a plurality of buffer regions, wherein said logic network writes and reads data from a plurality of data classes into said plurality of buffer regions such that each data class is written into and read from a different buffer region, and wherein said logic network increments a storage register associated with a buffer region each time that buffer region reaches a predetermined usage level; and

a timer for periodically sending a timing signal to said logic network;

wherein in response to said timing signal said logic network recalls data from said counter registers and re-partitions said buffer memory such that a more utilized buffer region is assigned more addressable memory registers.

9. (Original) A switch network according to claim 8 wherein said logic network assigns a buffer region that is used less often fewer addressable memory registers.

10. (Original) A switch network according to claim 8 wherein each buffer region is always assigned at least a minimum number of addressable memory registers.

11. (Original) A switch network according to claim 8 wherein said predetermined usage level is full.

12. (Previously Presented) A switch network according to claim 8 wherein when a least used buffer region is assigned a minimum number of addressable memory registers the logic network assigns a buffer region that is less often fully utilized but that has more than the minimum number of addressable memory registers.

13. (Original) A switch network according to claim 8 wherein said data classes represent virtual lanes.

14. (Previously Presented) A switch network according to claim 8 wherein said timing signal initiates clearing of said plurality of storage registers.

15. (Previously Presented) A switch network according to claim 8 wherein said card adaptor is a host channel adaptor.

16. (Previously Presented) A switch network according to claim 15 wherein said host channel adaptor is an Infiniband host channel adaptor.

17. (Previously Presented) A switch network according to claim 8 wherein said card adaptor is a target channel adaptor.

18. (Previously Presented) A switch network according to claim 17 wherein said host channel adaptor is an Infiniband host channel adaptor.

19. (Previously Presented) A switch network according to claim 8 further including a central processing unit for sending data to and receiving data from said memory device.

20. (Canceled) A method for managing a buffer comprising a plurality of addressable memory registers, comprising:

partitioning the buffer into the plurality of buffer regions controlled by hardware;

monitoring, with the hardware, usage of each buffer region within a time period; and

re-allocating the memory registers among the buffer regions with the hardware, based on the monitored usage.

21. (Canceled) The method of claim 20, further comprising associating each buffer region with a data class.

22. (Canceled) The method of claim 20, wherein at least one buffer region is associated with a data class representative of a virtual lane.